

FIG. 1A (Prior Art)

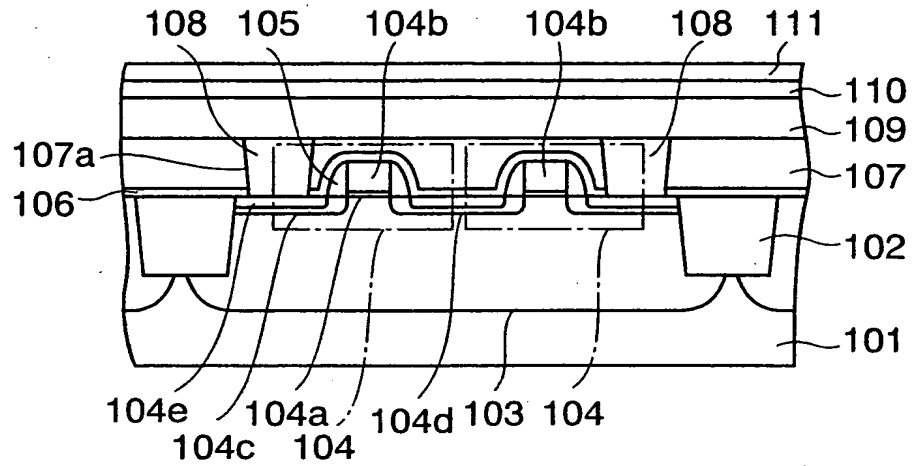


FIG. 1B (Prior Art)

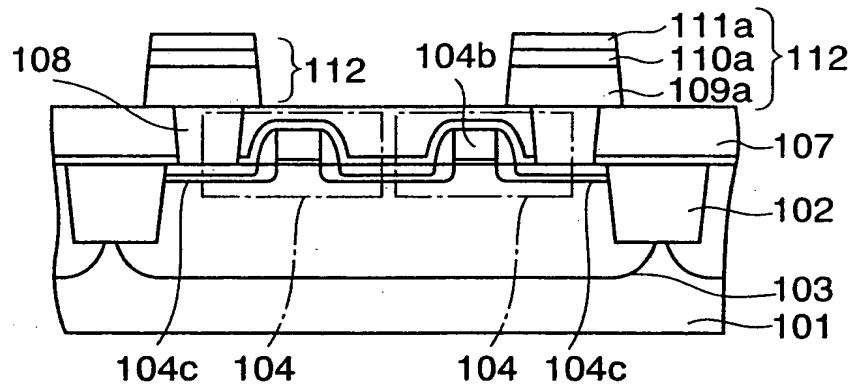


FIG. 1C (Prior Art)

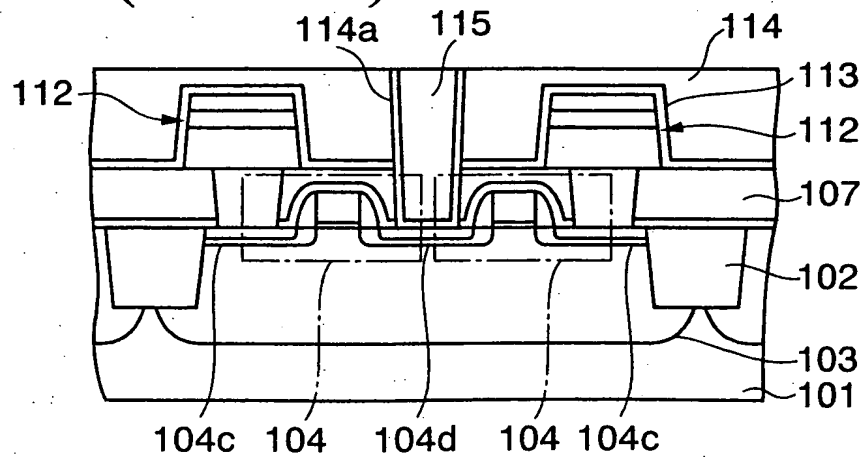


FIG. 1D (Prior Art)

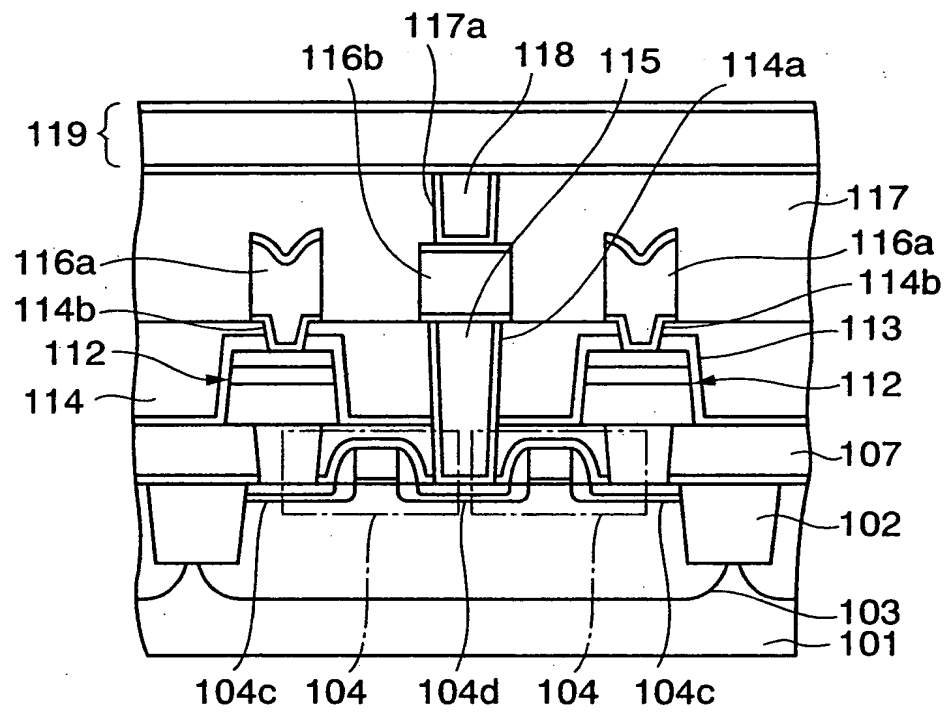


FIG. 2 (Prior Art)

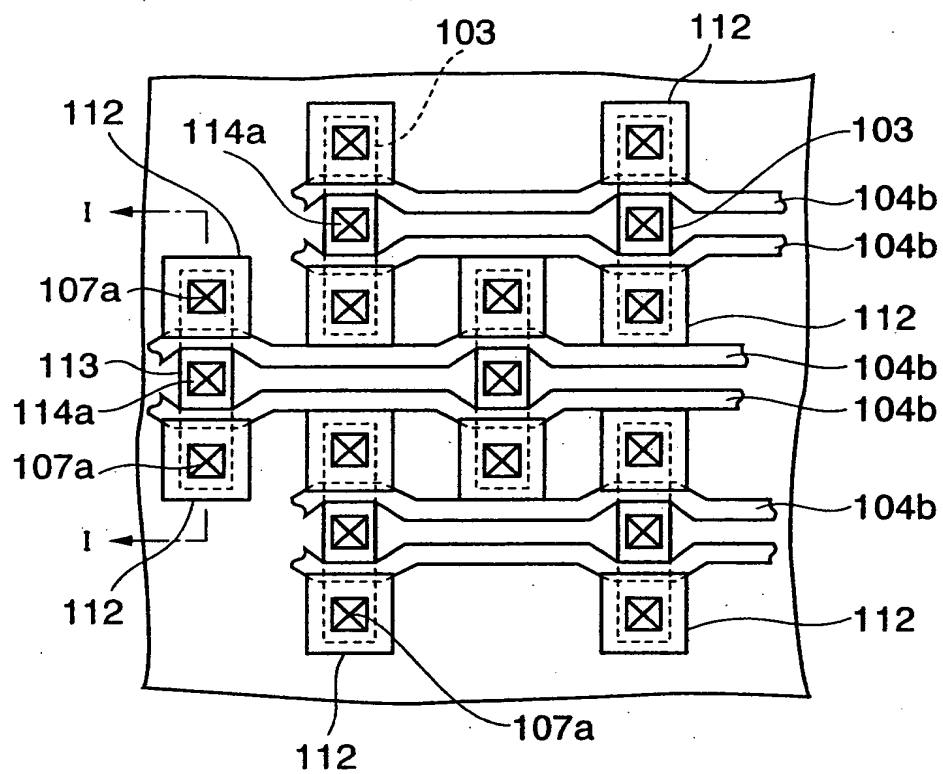


FIG. 3A

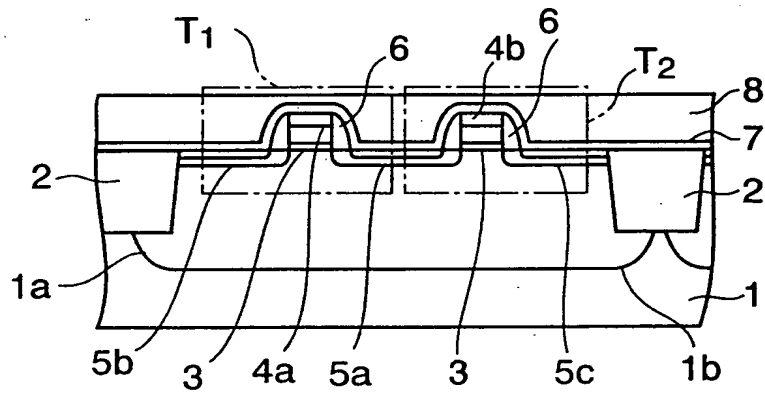


FIG. 3B

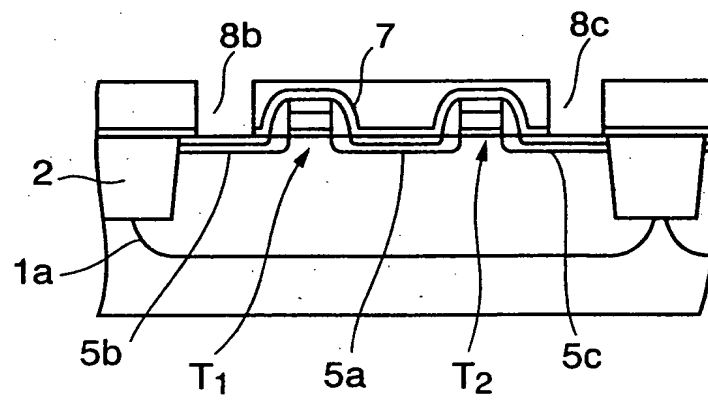


FIG. 3C

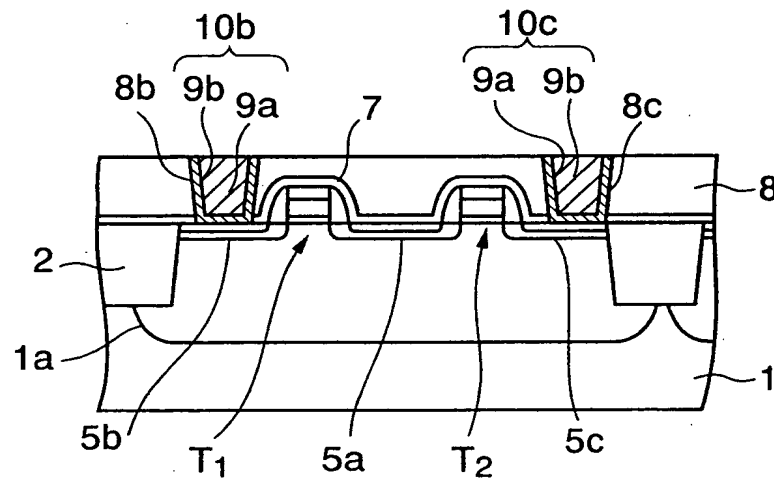


FIG. 3D

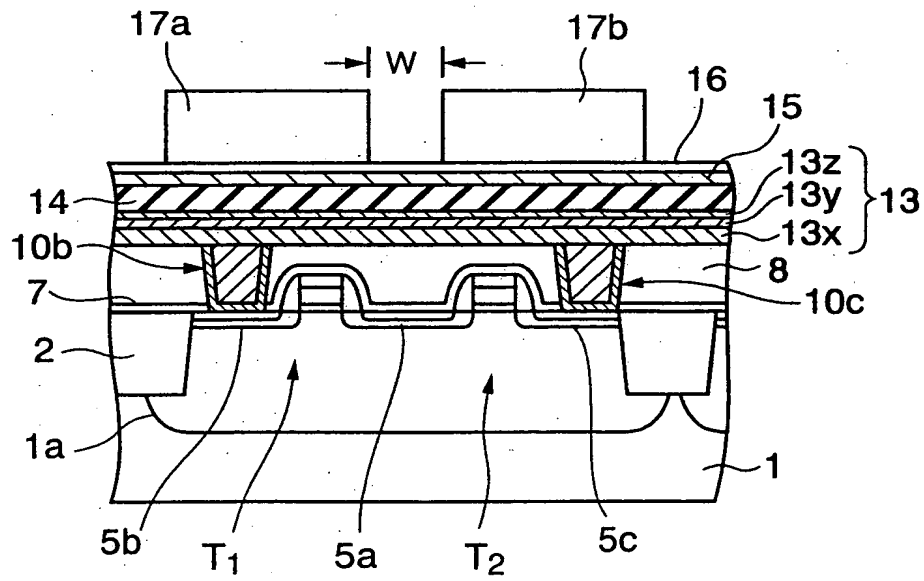


FIG. 3E

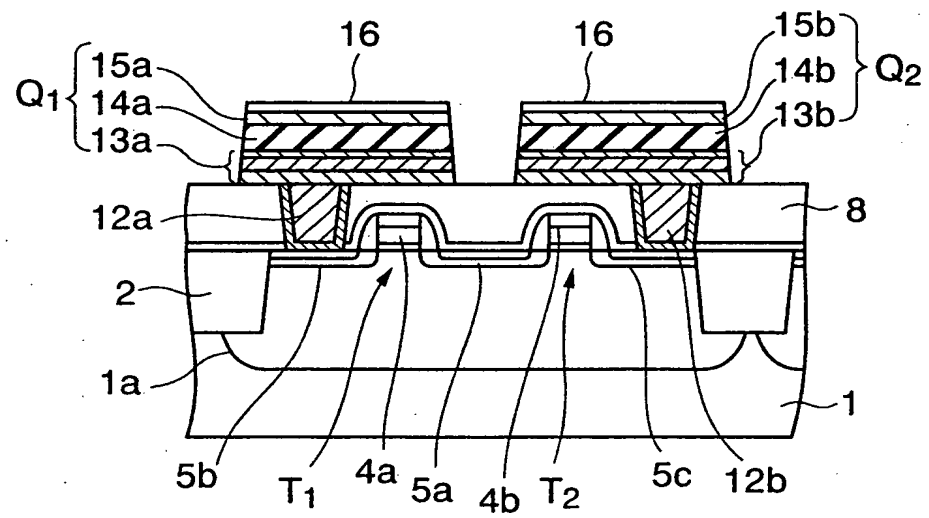
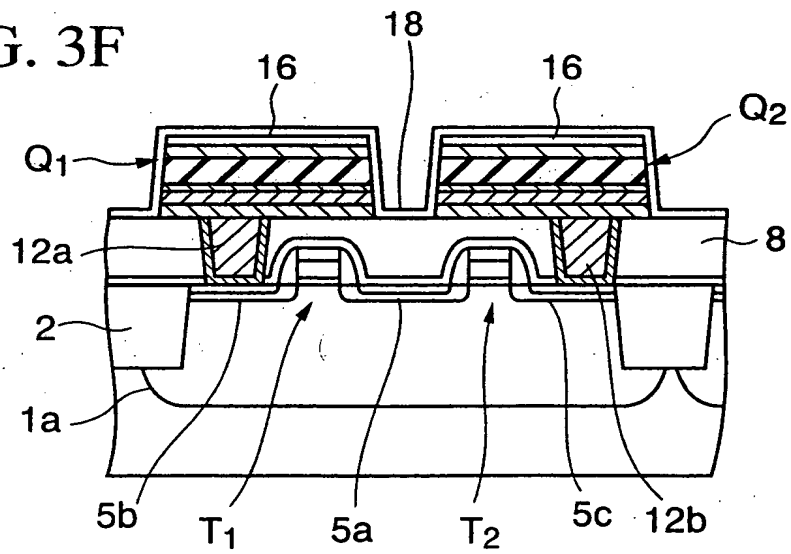


FIG. 3F



A cross-sectional view of a semiconductor device. It shows a substrate with a base layer 1a and a top layer 2. Two gates, 5a and 5b, are formed on the substrate. Gate 5a is labeled with T_1 and gate 5b with T_2 . The gates are separated by a region 5c. Above the gates, there are layers 7, 8, 12a, 12b, 18, 19, and 20. A layer 16 is also shown above the gates. Arrows point from the labels 5b, T_1 , 5a, T_2 , 5c, and 12b to their respective parts in the diagram.

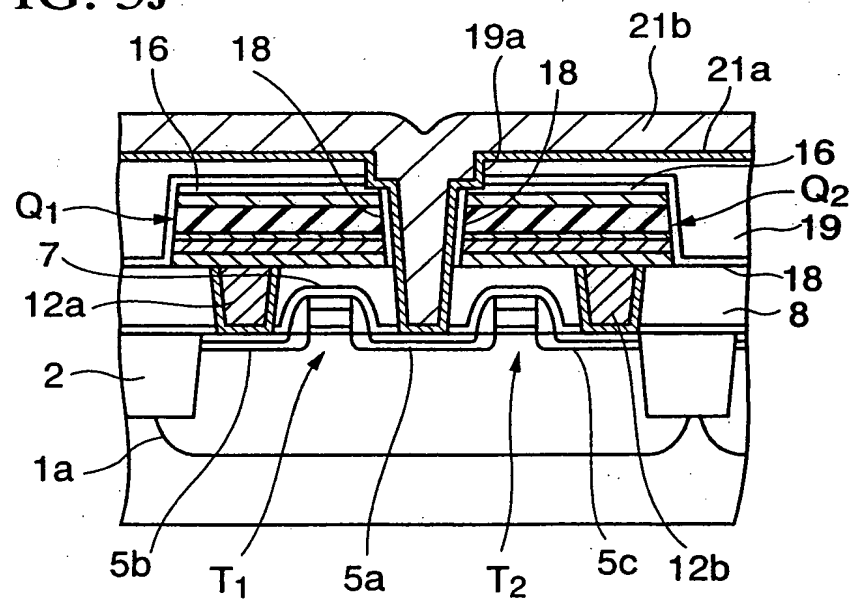


FIG. 3K

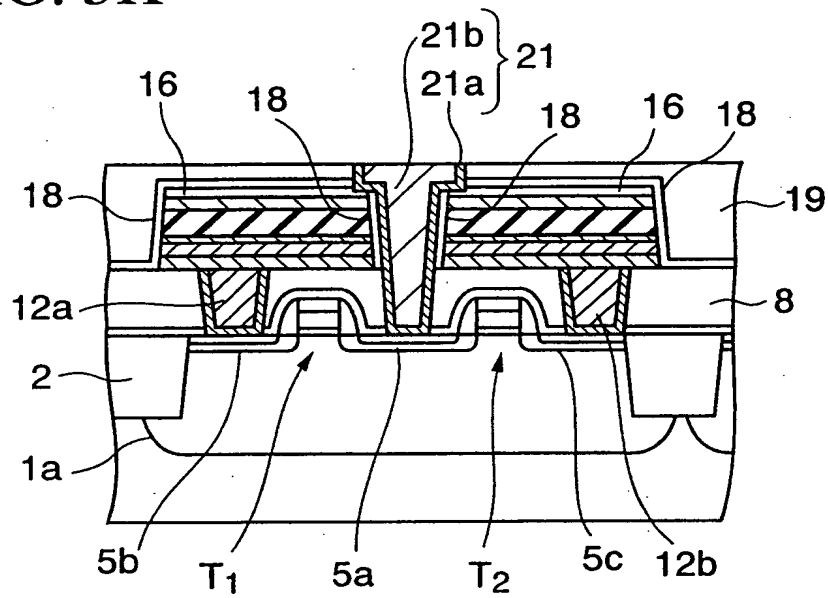
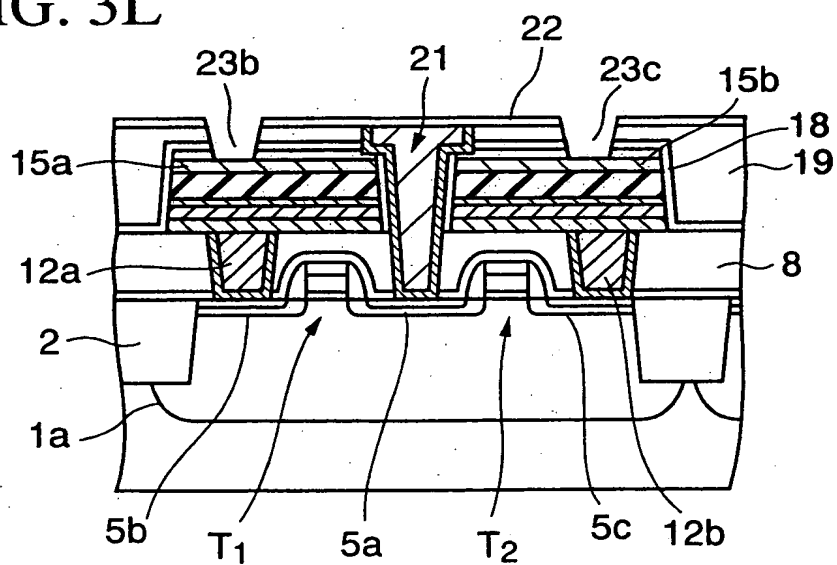


FIG. 3L



[illegible]

FIG. 4

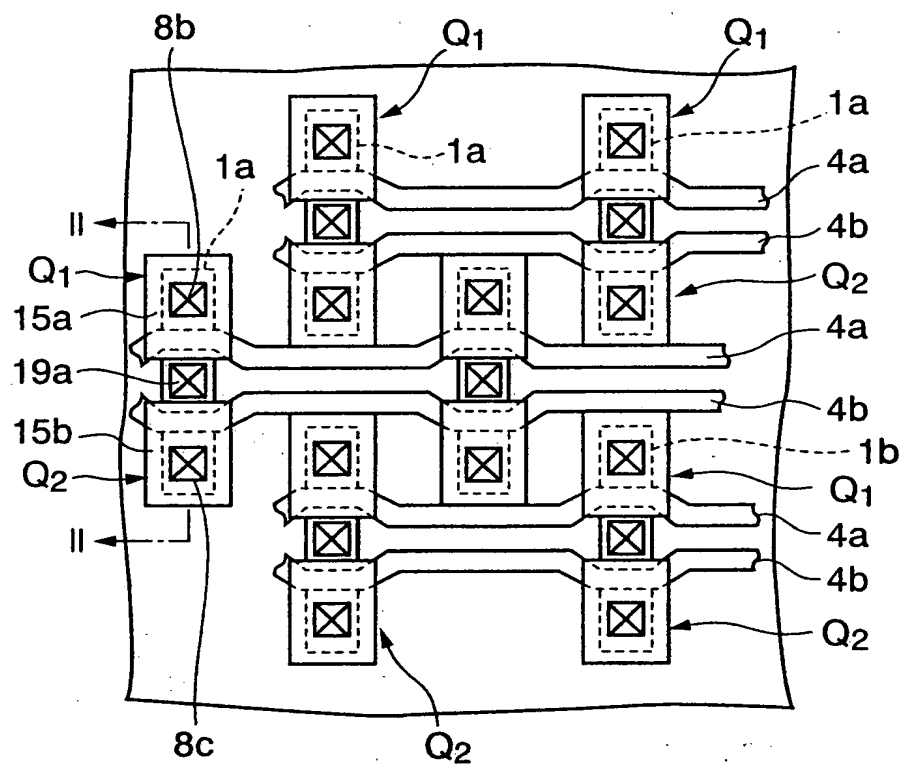


FIG. 5A

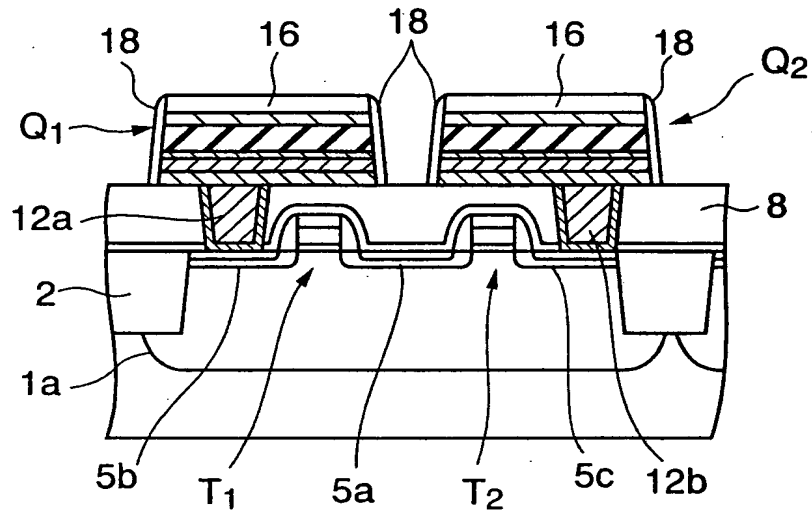


FIG. 5B

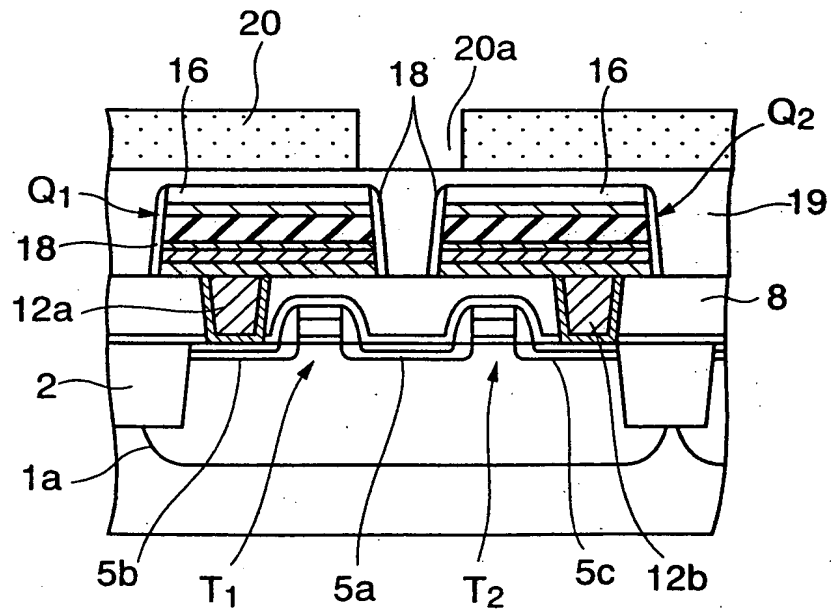


FIG. 5C

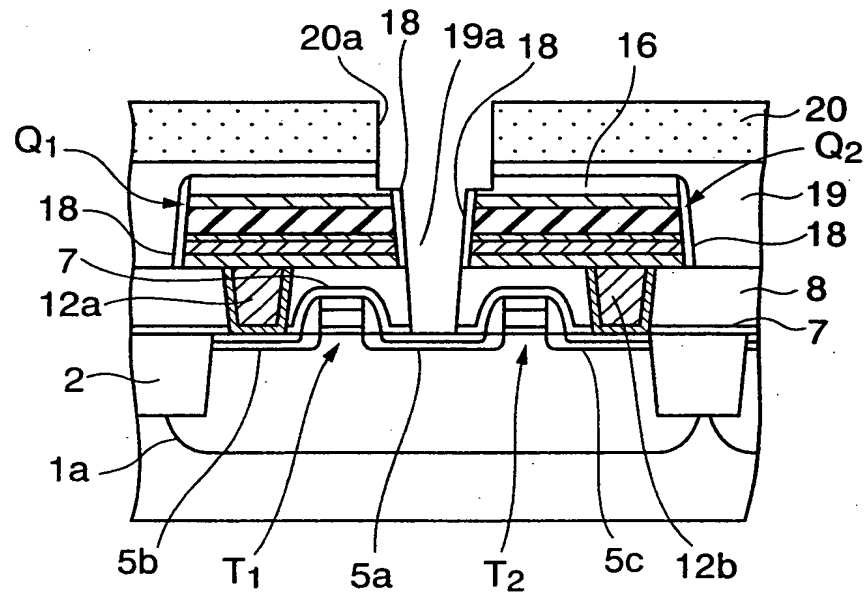


FIG. 5D

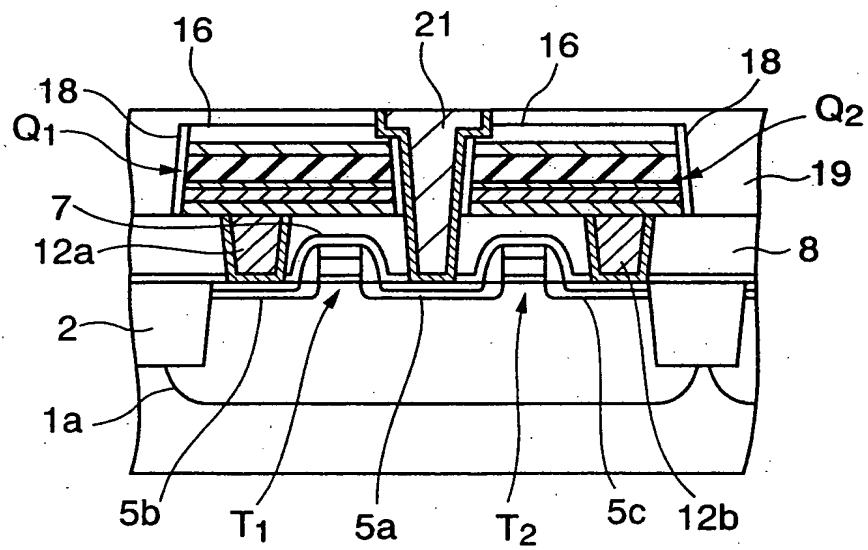


FIG. 5E

